Alternate Class AB Amplifier Design

This Class AB amplifier (Figure 1) has an integral common emitter bipolar amplifier (see Q4). The CE amplifier replaces the bipolar main amplifier in the previous design, i.e. Vs in this circuit is the output of the preamp. This produces a more compact and less expensive design since there are fewer components.

For designs with high open circuit gain, the overall voltage gain of the Class AB stage is determined by the feedback resistors R7 (R_A) and R5 (R_B). So \( A_V = -\frac{R_B}{R_A} \).

This audio amplifier has three aspects which need to be explained: (a) the VBE amplifier, (b) bootstrapping for increased gain, (c) feedback for output stability.
Figure 1. Alternate Class AB Amplifier Schematic
Amplifier Features

The VBE Multiplier

A V$_{BE}$ multiplier, sometimes called an amplified diode, (Figure 2) is used to provide a tunable voltage between the bases of the Darlington pairs X1 and X2. The purpose of this voltage is to bias the bases of the two Darlington pairs, keeping them in a "slightly" ON state - a quiescent current of about 20 mA is desirable. Tuning is obtained through the use of potentiometer XRV1. The quiescent current minimizes the zero crossing distortion associated with the power stage emitter followers. Since V$_{BE}$ is a function of temperature, Q3 should be mounted on the same heat sink as X1 and X2 to minimize voltage drift.

![Figure 2. Vbe Multiplier](image)

The value of the bias should be about $4 \times V_{BE} = 2.8V$, enough to forward bias each of the four base-emitter junctions in the pair of Darlington pairs.

Operation

Assume a current I flows down out of node 2. Assume the gain of Q3 is high, so
I_b3 can be ignored. A current I' = I - I_E flows through R1 and R2.

\[
V_{R1} = I'R1 \\
V_{R2} = I'R2 = \frac{R2}{R1}V_{BE3} \\
V(2,3) = V_{R1} + V_{R2} = \left(1 + \frac{R2}{R1}\right)V_{BE3}
\]

Thus the voltage drop is a multiple of \( V_{BE3} \), and is not restricted to being an integral multiple.

By placing a potentiometer at the base of Q3 we can adjust the bias to accommodate tolerance variations between Darlingtones. A capacitor can be used between nodes 2 and 3 to bypass ac signals so that the VBE multiplier provides a simple dc bias.

**Example 1**

Design a VBE multiplier to provide a 3.0 V bias. Assume \( I = 2.5 \) mA, \( \beta = 100 \), and \( V_{BE} = 0.7 \) V.

\[
V = \left(1 + \frac{R2}{R1}\right)V_{BE3} \\
R2 = \frac{V}{V_{BE3}} - 1 = \frac{3.0V}{0.7V} - 1 = 3.29
\]

Let the resistors have standard values \( R2 = 3.3 \, k\Omega \), \( R1 = 1.0 \, k\Omega \). Or we could let \( R2 \) be a 2.7 \, k\Omega fixed resistor and a 1 \, k\Omega potentiometer in series. This would allow bias adjustment from 2.59 V to 3.29 V.
CIRCUIT DESCRIPTION

*Spice extraction from McLogic
R2 2 1 3.3k
R1 1 0 1.0k
Q3 2 1 0 Q2N2222
I4 0 2 2.5mA
.lib eval.lib

DC Simulation of VBE Multiplier

BJT MODEL PARAMETERS

Q2N2222
NPN
IS 14.340000E-15
BF 255.9
NF 1
VAF 74.03
IKF .2847
ISE 14.340000E-15
NE 1.307
BR 6.092
NR 1
RE 10
RB 10
RBM 10
RC 1
CJE 22.010000E-12
MJE .377
CJC 7.306000E-12
MJC .3416
TF 411.100000E-12
XTF 3
VTF 1.7
ITF 1.6
TR 46.910000E-09
XTB 1.5

Note that since the 2N2222 transistor does not have the ideal V_{BE} of 0.7 V, the voltage drop across the V_{BE} multiplier is not exactly 3.0 V.
Note that in Example 1 the calculation produced the ratio of $R_2$ to $R_1$. How do you choose unique values? To get a better feel for the range of appropriate values, look at the ac resistance of the VBE multiplier:

$$r = \frac{R_2}{\beta} + \left(1 + \frac{R_2}{R_1}\right)r_e, \text{ where } r_e = \frac{0.025V}{I_c}$$

This can be derived from the ac equivalent circuit of the VBE multiplier. To produce a nearly pure dc voltage drop of a given value you would want $R_2$ small, $\beta$ large and $I_c$ large.

**Example 2**

*Calculate the ac resistance of the VBE multiplier in the previous example.*

$$I_E = I - I' = 2.5mA - \frac{0.7V}{1.0k\Omega} = 1.8mA$$

$$r_e = \frac{0.025V}{1.8mA} = 13.9\Omega$$

$$r = \frac{3.3k\Omega}{100} + \left(1 + \frac{3.3}{1.0}\right)13.9 = 33.0\Omega + 59.8\Omega = 92.8\Omega$$

*If this value of $r$ is too high you could lower $R_2$ (and $R_1$), raise $I$, or add a capacitor between nodes 2 and 3 with an impedance much less than $r$ at the frequencies of interest.*

**Bootstrapping**


Bootstrapping is a method of increasing the open loop [no feedback] gain of an
amplifier. In this amplifier, capacitor C4 is the bootstrap capacitor. The higher the open loop gain, the more accurately the equation $A_V = -\frac{R_b}{R_A}$ will predict the closed loop [with feedback] gain. Consider the circuit below, where $Q1$ is used in a common emitter amplifier and $Q2$ is an emitter follower (common collector amplifier).

If the ac voltage at the collector of $Q1$ is $v$, then voltage $A_V$ is present at the emitter of $Q2$ and also at the common terminals of $R3$ and $R4$, assuming that the impedance of $C4$ is very small at the frequencies of interest.

The gain $A$ of the common emitter amplifier is

$$A = \frac{R}{r_{e2} + R}, \text{ where } R = R_E || R3, \text{ and } r_{e2} = \frac{0.025V}{I_{c2}}$$

The voltage across resistor $R4$ is $v - A_V = (1 - A) \cdot v$.

So for ac signals, the resistance of $R4$ appears to be $R4' = R4 / (1 - A)$, which is much
higher than $R_4$ since $A$ is typically just slightly less than 1 for the emitter follower.

Since $R_4'$ is the collector resistance for the common emitter stage, the gain of the CE stage will become

$$A_V = -\frac{R_4' \parallel r_{\text{in(follower)}}}{r_{e1}}, \text{ where } r_{\text{in(follower)}} = r_\pi + (1 + \beta)R = \beta R$$

Without the bootstrapping, the gain would be

$$A_V = -\frac{(R_3 + R_4) \parallel r_{\text{in(follower)}}}{r_{e1}}$$

a value much less than that seen if $C_4$ is used.

**Example 3. Bootstrapping**

Design a CE/CC amplifier pair. Compare the voltage gains with and without bootstrapping.

**Assumptions and Design Parameters**

- $V_{cc} = 12 \text{ V}$
- $I_c$ for each transistor is $2.5 \text{ mA}$
- $\beta$ for each transistor is 100
- $R_L = 1 \text{ k}\Omega$
- Use 2N2222 for simulations

See appendix for detailed component calculations and PSpice files.
Without bootstrapping (Figure 4), the voltage gain is

\[
A_v = -\frac{RC \parallel (\beta \times RE2)}{r_{ei}} \times \frac{RE2}{RE2 + r_{e2}}, \text{ where } r_{ei} = \frac{V_t}{I_{ci}} = \frac{25\text{mV}}{I_{ci}}
\]

\[
A_v = -\frac{1.6k\Omega \parallel 290k\Omega}{10\Omega} \times \frac{2.9k\Omega}{2.9k\Omega + 10\Omega}
\]

\[
A_v = -159 \times \frac{2900}{2910} = -158.6
\]

\[
A_v (\text{PSpice}) = -129
\]

\(\beta \times RE2\) represents the input resistance of the common collector amplifier, and is the load for the common emitter amp.

With bootstrapping (Figure 5), the collector resistor of the common emitter is split into two pieces and the bootstrap capacitor \(C4\) is
added. The impedance of C4 should be small in the audio frequency band.

Figure 5. Common emitter, common collector amplifiers with bootstrapping. RC was split in half and capacitor C4 added. The amplitude of the sine wave input was reduced in anticipation of higher gain.

The voltage gain of the amplifier pair is $A_v$, and the voltage gain of the common collector stage is $A$.

$$A_v = \frac{-RC2' || r_{in}(\text{follower})}{r_{ei}} \times A$$

where $r_{ei} = \frac{V_t}{I_{ci}} = \frac{25\text{mV}}{I_{ci}}$, $A = \frac{R}{R + r_{e2}}$, $R = RE2 || RC1$, and $r_{in}(\text{follower}) = \beta R$
Plug in the component values and solve for the bootstrap gain:

\[ R = RE2 \parallel RC1 = 2.9k\Omega \parallel 800\Omega = 627\Omega \]

\[ r_{e2} = \frac{25mV}{2.5mA} = 10\Omega \]

\[ A = \frac{R}{R + r_{e2}} = \frac{627\Omega}{637\Omega} = 0.984 \]

\[ RC2' = \frac{RC2}{1 - A} = \frac{800\Omega}{1 - 0.984} = 50k\Omega \]

\[ A_v = -\frac{50k\Omega \parallel 62.7k\Omega}{10\Omega} \times 0.984 \]

\[ A_v = -2782 \times 0.984 = -2737 \]

\[ A_v (\text{PSpice}) = -1300 \]

While we can show a large increase in gain (factor of nearly 20) from the no bootstrap case, the calculation and simulation do not match. The reason for this is not yet known.
Appendix

Amplifier Calculations

$I_c = 2.5 \text{ mA}, \beta = 100, R_L = 1\text{k} \Omega, V_{cc} = 12 \text{ V}.$

Let the voltage at the base of $Q_1$, $V_B$, be about $V_{cc}/3$ or 4 V for good output swing.

Then at the emitter of $Q_1$, $V_E = 4 - V_{BE} = 3.3 \text{ V}$.

Let $I_E = I_C$ to simplify calculations.

$$R_{E1} = \frac{V_E}{I_E} = \frac{3.3 \text{ V}}{2.5 \text{ mA}} = 1.32 \text{k} \Omega$$

Let the current through the divider consisting of $R_1$ and $R_2$ be about ten times the $Q_1$ base current, or about $0.1I_E$ when $\beta = 100$.

$$R_1 + R_2 = \frac{12 \text{ V}}{0.25 \text{ mA}} = 48 \text{k} \Omega$$

$$\frac{R_2}{R_1 + R_2} \frac{V_{cc}}{V_{bc}} = 4 \text{ V}$$

$$R_2 = \frac{4 \text{ V}}{V_{cc}} (R_1 + R_2) = \frac{4 \text{ V}}{12 \text{ V}} 48 \text{k} \Omega = 16 \text{k} \Omega$$

$$R_1 = 32 \text{k} \Omega$$

Let the drop across $Q_1$'s collector resistor be about $V_{cc}/3$.

$$R_C = \frac{V_{cc} - V_c}{I_c} = \frac{4 \text{ V}}{2.5 \text{ mA}} = 1.6 \text{k} \Omega$$

The dc bias at the base of $Q_2$ should be 8 V. The emitter voltage should be 7.3 V.
\[ \frac{7.3V}{2.5mA} = 2.9k\Omega \]

**PSpice Input Files**

CE/CC Amplifier - no bootstrapping
* nominal gain = -160
* Spice extraction from McLogic

```
C1     1 b1  91uF
C2     e2  Vout  33uF
RC     Vcc  c1  1.6k
RE1    e1  0  1.32k
RE2    e2  0  2.9k
Vin    Vin  0  sin(0V 10mV 1kHz)
Vcc    Vcc  0  12V
Q1     c1  b1  e1  Q2N2222
CE     e1  0  1000uF
R1     Vcc  b1  32k
R2     b1  0  16k
RL     Vout  0  1k
Q2     Vcc  c1  e2  Q2N2222
Rs     Vin  1  100
* Pull the transistor models from the eval library
.lib eval.lib
.probe
* Run simulation for 2 cycles, 200 points minimum
.tran 0.02ms 2ms 0 10us
* Show the output voltage in the dialog box as sim runs
.watch tran V([Vout])
.end
```

Bootstrapped CC/CE amplifier
* Nominal gain = -2700
* Spice extraction from McLogic

C1     1 b1  91uF
C2  e2  Vout  33uF
RC1  Vcc  2  800
RC2  2  c1  800
RE1  e1  0  1.32k
Vin  Vin  0  sin(0V 1mV 1kHz)
Vcc  Vcc  0  12V
Q1  c1  b1  e1  Q2N2222
CE  e1  0  1000uF
R1  Vcc  b1  32k
R2  b1  0  16k
RL  Vout  0  1k
Q2  Vcc  c1  e2  Q2N2222
RE2  e2  0  2.9k
Rs  Vin  1  100
C4  2  e2  4000uF

* Pull the transistor models from the eval library
.lib eval.lib
.probe
* Run simulation for 2 cycles, 200 points minimum
.tran 0.02ms 2ms 0 10us
* Show the output voltage in the dialog box as sim runs
.watch tran V([Vout])
.end