

## **ECE Laboratory IV Spring 2006**

**Instructor** – Eric Gallo  
[eg@ece.drexel.edu](mailto:eg@ece.drexel.edu)  
Bossone 502  
x1378  
Office Hours – Wednesday 5:00-6:00pm by appointment

### **Overview**

Over these ten weeks we will construct and test a digital recording system. Our circuit is similar to a data acquisition system. Its function is to record a portion of an analog signal and then play it back. The circuit consists of an analog to digital converter (ADC) front end, an 128k x 8 RAM chip, and a digital to analog converter (DAC). Associated circuitry includes an on-board timer, address generation, and read/write control. We will supplement the circuit construction with two PSpice simulations which will develop some basic understanding of the circuits involved. This project will take the entire 10 weeks of the term.

There are seven steps in the circuit project. Some steps have pre-lab assignments. All steps have tasks and deliverables. A detailed timeline is available on the course web site.

- Step 1 Review of ADC and DAC - simulation
- Step 2 Building the ADC Circuit - hardware
- Step 3 Build the DAC Circuit - hardware
- Step 4 Introduce Static RAM - simulation
- Step 5 Build the On-Board Clock - hardware
- Step 6 Introduce Control Logic Functionality - hardware
- Step 7 Final Changes - hardware

### **Course Goals**

- \* Provide a practical experience in circuit prototyping
- \* Integrate analog and digital circuit design concepts
- \* Further develop student's OrCAD/PSpice circuit simulation expertise
- \* Emphasize the Logic Analyzer as a diagnostic tool
- \* Incorporate system-level and scheduling considerations into design

### **Course Format**

We have a one hour common lecture and a two hour lab period each week of the term. In some cases work will be required outside of the regularly scheduled hours for circuit construction and testing. Copies of the lectures will be placed on the course web site for review.

### **Expectations of Students and Staff**

What is expected of you?

- \* Attendance in lab lecture
- \* Attendance in lab hours

You can work in a group of 2, but reports will be done individually

You will attend the lab section listed on your schedule

- \* 2 to 3 hours of work outside of lab
- \* Assignments will be turned in on time
- \* You will maintain a bound lab notebook that will be turned in no later than Monday of Finals Week.

What is expected of us?

- \* We will provide you with the materials and documentation needed to perform the project
- \* We will provide grade feedback on a timely basis. These grades will be available on the course web site.

### **Grading Basis**

The grading basis is 90% laboratories, 10% quizzes. The deliverables for each Step of the project will receive a numerical grade. The grades for steps which involve circuit design and construction will have several parts, including design, functionality, quality of construction. Steps 2 and 6 are multi-week experiments, and will receive heavier weight.

Deliverables are due no later than one week after your scheduled lab meeting. Reports which are late will lose 10% in value per week until four weeks have gone by, at which time the report will not be accepted. All materials (hardware and reports) must be received by the first day of finals week. After this time, they will not be accepted.

### **Academic Honesty Policy**

The University policies on academic honesty will be enforced. The full description of the University academic honesty policy and remedies is listed in the Student Handbook, Section 10. Academic Honesty. The handbook is available on the web at <http://www.drexel.edu/studentlife/studenthandbook/>.

### **Students Needing Accommodations**

Students have the right to receive accommodations if they have registered with the Drexel Office of Disability Services (215 Creese Student Center, 215-895-2506/7) and have submitted an Accommodation Verification letter to their professor. You should arrange a meeting with your professor privately during office hours to discuss your needs.